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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/706,043	KAJITA ET AL.
	Examiner	Art Unit
	Alexander O. Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/706043 Attorney's Docket #: 24533US2S
Filing Date: 11/13/2003; claimed foreign priority to 7/30/2003

Applicant: Kajita et al.

Examiner: Alexander Williams

Applicant's election of the species of figures 1 to 7 (claims 1 to 9), filed 12/13/04, has been acknowledged.

This application contains claims 10 to 19 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the the first intervention conductive film consists substantially of a material selected from the group consisting of Ti, TiN and TiSiN or a stacked film containing a combination thereof, and the buried conductive film consists substantially of a material selected from the group

consisting of TiN, TiSi,N, Ta and TaN or a stacked film containing a combination thereof in claim 6 and wherein the buried conductive film and the first intervention conductive film consist substantially of a material selected from the group consisting of TiN and TiSiN or a combination thereof in claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 5 and 6 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is unclear and confusing to what is meant by and what shows all the different combinations of "wherein the buried conductive film and the first intervention conductive film consist substantially of a material selected from the group consisting of TiN and TiSiN or a combination thereof." Where are these combination shown in the drawings or detailed in the specification?

In claim 6, it is unclear and confusing to what is meant by and what shows all the different combinations of "the first intervention conductive film consists substantially of a material selected from the group consisting of Ti, TiN and TiSiN or a stacked film containing a combination thereof, and the buried conductive film consists substantially of a material selected from the group consisting of TiN, TiSi,N, Ta and TaN or a stacked film containing a combination thereof." Where are these combination shown in the drawings or detailed in the specification? Claim 7 recite alternative structures.

Any of claims 5 and 6 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a buried conductive film; first intervention conductive films; and an interconnect trench and the buried conductive film and the conductive plug deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 4 and 7 to 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe (U.S. Patent Application Publication # 2004/0021227 A1).

1. Watanabe (figures 1 to 38) specifically figure 31 show a semiconductor device comprising: a semiconductor substrate **100**; an active element structure **104,106** formed on the semiconductor substrate, and having a connection region formed in the surface of the semiconductor substrate; a first insulating film **108** provided on the semiconductor substrate; a contact hole **(hole in which 110 resides)** extending from a surface of the first insulating film to the connection region; a contact plug **(material 110 within the contact hole)** provided in the contact hole; and a buried conductive film **114** filled in a clearance formed in the contact plug, consisting of a material different from the contact plug, and having a continuous surface without forming a step with the surface of the contact plug.

2. The device according to claim 1, Watanabe further comprising: a barrier metal **110** provided in an interconnect trench formed on the contact plug and the buried conductive film, and having a bottom surface common to the upper surface of the contact plug and the buried conductive film; and an interconnect layer provided in the interconnect trench, and consisting of a conductive material.

3. The device according to claim 1, Watanabe further comprising: a first intervention conductive film interposed between the inner surface of the contact hole and the contact plug.

4. The device according to claim 3, Watanabe show wherein the buried conductive film and the first intervention conductive film consist of substantially the same material.

7. The device according to claim 2, wherein a film thickness of the first intervention conductive film is equal to or less than 10% of the width of cross section of the interconnect trench.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. The device according to claim 1, Watanabe show wherein the active element structure includes a transistor.

9. The device according to claim 1, Watanabe show wherein the contact plug consists substantially of W.

Therefore, it would have been obvious to one of ordinary skill in the art to use the **buried conductive film; first**

<u>intervention conductive films; and an interconnect trench</u> as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 1 to 9, **insofar as claim 6 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi et al. (U.S. Patent # 6,576,512 B2).

1. Taniguchi et al. (figures 1 to 62) specifically figures 44 to 53 show a semiconductor device comprising: a semiconductor substrate **1**; an active element structure **12s,12d,9w** formed on the semiconductor substrate, and having a connection region formed in the surface of the semiconductor substrate; a first insulating film **23,24** provided on the semiconductor substrate; a contact hole **24h** extending from a surface of the first insulating film to the connection region; a contact plug provided in the contact hole; and a buried conductive film filled in a clearance formed in the contact plug, consisting of a material different from the contact plug, and having a continuous surface without forming a step with the surface of the contact plug.

2. The device according to claim 1, Taniguchi et al. further comprising: a barrier metal **31** provided in an interconnect trench formed on the contact plug and the buried conductive film, and having a bottom surface common to the upper surface of the contact plug and the buried conductive film; and an interconnect layer provided in the interconnect trench, and consisting of a conductive material.

3. The device according to claim 1, Taniguchi et al. further comprising: a first intervention conductive film **31** interposed between the inner surface of the contact hole and the contact plug.

4. The device according to claim 3, Taniguchi et al. show wherein the buried conductive film **31** and the first intervention conductive film **31** consist of substantially the same material.

5. The device according to claim 4, Taniguchi et al. show wherein the buried conductive film **31** and the first intervention conductive film **31** consist substantially of a material selected from the group consisting of **TiN** and TiSiN or a combination thereof.

6. The device according to claim 3, Taniguchi et al. show wherein the first intervention conductive film **31** consists substantially of a material selected from the group consisting of Ti, **TiN** and TiSiN or a stacked film containing a combination thereof, and the buried conductive film **31** consists substantially of a material selected from the group

consisting of **TiN**, TiSi,N, Ta and TaN or a stacked film containing a combination thereof.

7. The device according to claim 2, Taniguchi et al. show wherein a film thickness of the first intervention conductive film is equal to or less than 10% of the width of cross section of the interconnect trench.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. The device according to claim 1, Taniguchi et al. show wherein the active element structure includes a transistor.

9. The device according to claim 1, Taniguchi et al. show wherein the contact plug consists substantially of W.

Therefore, it would have been obvious to one of ordinary skill in the art to use the **buried conductive film; first intervention conductive films; and an interconnect trench** as "merely a matter of obvious engineering choice" as set forth in the above case law.

DOCUMENT-IDENTIFIER: US 6,576,512 B2
TITLE: Semiconductor integrated circuit device and a method of manufacturing the same

Detail Description Paragraph - DETX (97):
[0283] First, plugs P1 are formed to fill the contact holes TH. The plugs P1 are tungsten plugs formed as described below.

Detail Description Paragraph - DETX (98):
[0284] Titanium nitride (TiN) is thinly deposited using sputtering as a reaction preventing film for preventing any reaction between tungsten and the underlying salicide layers. Next, tungsten (W) is deposited on the titanium nitride films to fill the contact holes TH. In order to fill the contact holes TH with tungsten (W) completely, the tungsten must have a thickness which is equal to or greater than one half of the diameter of the contact holes.

Thereafter, a method is employed to etch the deposited tungsten (W) and titanium nitride (TiN) as a whole (etch back) to leave the plugs P1 only in the contact holes.

Detail Description Paragraph - DETX (99):
[0285] Next, a metal layer is deposited using sputtering and is patterned into first layer wiring by means of the well known photolithography utilizing a photoresist pattern as a mask. The first wiring layer is constituted by TiN, Ti, AlCu and Ti (a top layer, upper layer, main wiring layer and bottom layer). Specifically, the first wiring layer is multi-layer wiring formed by sequentially sputtering Ti (with a thickness of 10 nm) at the bottom to provide adhesion to the .sub.SiO2 film (layer insulation film) and to reduce contact resistance with the tungsten plugs, Al-0.5% Cu (with a thickness of 500 nm), aluminum being the primary wiring material, Ti (with a thickness of 10 nm) to improve adhesion between AlCu and TiN and TiN (with a thickness of 75 nm) as a reflection preventing film. The reflection preventing film (TiN) is a film for preventing the photoresist from being overexposed to light reflected by the metal layer during the exposure of the photoresist.

Detail Description Paragraph - DETX (101):
[0287] As shown in FIG. 29, a second wiring layer M2 is patterned on a layer insulation film 23, the layer M2 being connected to the first wiring layer M1 through plugs P2.

Detail Description Paragraph - DETX (105):
[0291] As shown in FIG. 30, a third wiring layer M3 is patterned on a layer insulation film 24, the layer M3 being connected to the second wiring layer M2 through plugs P3.

Detail Description Paragraph - DETX (108):
[0294] As shown in FIG. 31, a fourth wiring layer M4 is patterned on a layer insulation film 25, the layer M4 being connected to the third wiring layer M3 through plugs P4.

[0364] As shown in FIG. 44, bit lines BL are formed through plugs P1 filled in the contact holes TH.

Detail Description Paragraph - DETX (179):
[0365] First, a polycrystalline silicon layer including an n-type impurity (doped polysilicon) is deposited to fill the contact holes TH, and the plugs P1 are formed through a process

of etching the polycrystalline silicon layer as a whole, i.e., a so-called etch-back process. CMP may be used for the formation of the plugs P1. The use of CMP is rather recommendable to prevent recession of the plugs P1 attributable to over-etching.

Detail Description Paragraph - DETX (180):
[0366] Subsequently, the bit lines BL are formed on the layer insulation film 23. The bit lines BL are formed by depositing a TiN film and a W film on the layer insulation film 23 using sputtering, depositing a silicon nitride film (not shown) on the W film using CVD and thereafter patterning those films through etching utilizing a photoresist pattern as a mask.

Detail Description Paragraph - DETX (183):
[0369] Subsequently, an opening 24h is provided on the layer insulation film by means of etching to expose the surface of the plug P1 to which a capacitor is to be connected using a photoresist pattern PR101 as a mask.

Detail Description Paragraph - DETX (184):
[0370] Next, as shown in FIG. 46, a lower electrode (accumulation electrode) 30 is formed along the side wall of the opening 24h. The accumulation electrode 30 is formed by depositing a W film using CVD or sputtering and by patterning it by means of etching utilizing a photoresist pattern as a mask. Next, an insulation film (dielectric film) 31 is formed on the exposed surface of the lower electrode 30.

Detail Description Paragraph - DETX (185):
[0371] For example, the capacitor insulation film 30 is made of tantalum oxide (Ta.sub.2O.sub.5) having a relatively high dielectric constant. The tantalum oxide film 31 is formed by depositing amorphous tantalum oxide to a thickness of about 20 nm using CVD and by thereafter performing a thermal oxidation process to crystallize the tantalum oxide. Then, an upper (plate) electrode 31 for the capacitor insulation film is formed. The upper (plate) electrode 31 is constituted by a TiN film formed using sputtering.

Detail Description Paragraph - DETX (186):
[0372] While a tantalum oxide film is used as the capacitor insulation film, other metal oxide films, e.g., a high dielectric film such as (Ba, Sr) TiO3 film or Pb (Zr, Ti) 03 film may be used. While a TiN film is used to form the

plate electrode, a metal film having a refractory metal film selected from among a group including a tungsten nitride (WN) film and a tungsten (W) film.
In addition, the plate electrode may be a polycrystalline silicon film including an impurity. When a polycrystalline silicon film is used, the surface of the polycrystalline silicon film is also silicidized at a step of forming a silicide layer to be described later to reduce the resistance of the plate electrode.

Detail Description Paragraph - DETX (187):
[0373] (Step of Forming Side Wall Spacers of PMOS Gate Electrodes)

Detail Description Paragraph - DETX (189):
[0375] Next, as shown in FIG. 48, the exposed silicon nitride film 15 is subjected to reactive ion etching (anisotropic etching) to form side wall spacers 15don the side walls of the NMOS gate electrode 9a.

Detail Description Paragraph - DETX (191):
[0377] Subsequently, as shown in FIG. 48, high concentration regions 19s and 19d aligned by the side wall spacers 15d are formed. Specifically, ion implantation is carried out to introduce a p-type impurity, e.g., boron (B)
into the nwell 4a such that it is defined by the side wall spacers 15d. For example, the ion implantation is carried out with an acceleration energy at 10 KeV and in a dose of about 3.times.10.sup.15 atoms/cm. During the ion implantation, the impurity is also introduced into the gate electrode 9a provide a p-gate (gate electrode of the p conductivity type) PMOS.

Detail Description Paragraph - DETX (192):
[0378] (Step of Forming Side Wall Spacers of NMOS Gate Electrodes)

Detail Description Paragraph - DETX (194):
[0380] Next, as shown in FIG. 50, the exposed silicon nitride film 15 is subjected to reactive ion etching (anisotropic etching) to form side wall spacers 15don the side walls of the PMOS gate electrode 9a.

Detail Description Paragraph - DETX (196):

[0382] Subsequently, as shown in FIG. 50, high concentration regions 16sand i6d aligned by the side wall spacers 15d are formed. Specifically, ion implantation is carried out to introduce an n-type impurity, e.g., arsenic (As) into the p-well such that it is defined by the side wall spacers 15d. For example, the ion implantation is carried out with an acceleration energy at 60 KeV and in a dose of about 3.times.10.sup.15 atoms/cm.sub.2. The ion implantation introduces the impurity to also each of the gate electrodes 9b and 9e to provide n-gate (gate electrodes of the n-conductivity type) NMOSs.

Detail Description Paragraph - DETX (198):
[0384] As shown in FIG. 51, a metal-semiconductor reaction layer (salicide layer) is formed on the gate electrodes in the high speed logic portion (NMOS and PMOS) and the surface of the high concentration regions. Specifically, a cobalt suicide layer is formed using the same silicidation technique as in the first embodiment. Although not shown, when cobalt is deposited prior to the silicidation, the surface of the plate electrode 32 is protected by an insulation film such as a silicon oxide film. As a result, the cobalt silicide layer of the NMOS is formed in alignment with the side wall spacers 15a formed in the high concentration region. The cobalt silicide layer of the PMOS is formed in alignment with the side wall spacers 15a formed in the high concentration region.

Detail Description Paragraph - DETX (199):
[0385] When a polycrystalline silicon film is used as the plate electrode as described above, there is no need for an insulation film on the surface of the plate electrode to protect the same. In the case, cobalt is also deposited on the surface of the plate electrode 32. A cobalt silicide layer may be formed on the surface of the plate electrode 32 at the same time when the cobalt silicide layer on the gate electrode and the surface of the high concentration regions.

Detail Description Paragraph - DETX (203):
[0389] Next, plugs P1 are formed to fill the contact holes TH. The plugs P1 are tungsten plugs which are formed in the following procedure. First, sputtering is performed to thinly deposit titanium nitride (TiN) as a reaction preventing film for preventing reaction between tungsten and the underlying salicide layers. Subsequently, tungsten (W) is deposited on the titanium nitride film to fill the contact holes TH. A process

(etch back) is performed to etch the deposited tungsten (W) and titanium nitride (TiN) as a whole to leave the plugs P1 in the contact holes TH.

Detail Description Paragraph - DETX (204):
[0390] Next, a metal layer is deposited, and a first wiring layer is formed using a well known technique utilizing a photoresist pattern as a mask. For example, the metal layer serving as wiring is constituted by TiN, Ti, AlCu and TiN (a top layer, upper layer, main wiring layer and bottom layer) as in the first embodiment. Specifically, the first wiring layer is multi-layer wiring formed by sequentially sputtering Ti (with a thickness of 10 nm) at the bottom to provide adhesion to the .sub.SiO2 film (layer insulation film) and to reduce contact resistance with the W plugs, Al-0.5% Cu (with a thickness of 500 nm), aluminum being the primary wiring material, Ti (with a thickness of 10 nm) to improve adhesion between AlCu and TiN and TiN (with a thickness of 75 nm) as a reflection preventing film.

Detail Description Paragraph - DETX (207):
[0393] Subsequently, contact holes TH are provided on the silicon oxide film 29 to expose a part of the first wiring layer M1. A metal layer is then deposited, and a second wiring layer M2 is formed using a well known technique utilizing a photoresist pattern as a mask. For example, the metal layer serving as wiring is constituted by TiN, Ti, AlCu and TiN (a top layer, upper layer, main wiring layer and bottom layer) as in like the first wiring layer.
Since the layer insulation film 29 is planarized using CMP as illustrated, for example, the second wiring layer M2 may be extended on to the DRAM cell portion (DRAM memory array) to interconnect the circuit blocks. Since the freedom in arranging circuit blocks in a semiconductor chip is thus increased, it is possible to provide a system LSI incorporating a DRAM suitable for a high speed operation. The term "circuit blocks" represents the DRAM memory array DMAY, input/output control portion I/O, high speed logic circuit portion LOGIC and the like.

Detail Description Paragraph - DETX (211):
[0397] Further, CMISs having a dual gate structure constituted by a p-gate PMOS and an n-gate .NMOS is provided, which makes it possible to provide a high performance system LSI incorporating a DRAM in which fineness is achieved and

short channel effects are suppressed.

Detail Description Paragraph - DETX (212):
[0398] Further, the DRAM cell portion is formed by CMOSs having a polycide gate structure and the high speed logic portion is formed by CMOSs having a salicide gate structure. This makes it possible to provide a system LSI incorporating a DRAM at a high level of integration which achieves a higher speed and lower power consumption at the same time.

Detail Description Paragraph - DETX (213):
[0399] In each of the above-described embodiments, the PMOS and NMOS gate insulation films are not limited to single-layer films constituted by an oxide film (specifically a silicon oxide film). Depending on needs in view of improvement of device characteristics and reliability, they may be multi-layer films formed by a nitride film (specifically a silicon nitride) and an oxide film, composite films referred to as "oxinitride films" or single-layer films constituted by a nitride film.

Detail Description Paragraph - DETX (225):
[0411] Etching is carried out on the SiO.sub.2 film (silicon oxide film) 115 using the first pattern mask PR11. As a result, the film is removed from the top of the gate electrodes 9b and 9e, and side wall films 15a and 15b (first gate insulation films) are left on the side walls of the gate electrodes 9b and 9e. The SiO.sub.2 film 115 is selectively etched on the side walls of the gate electrode 9d with the first pattern mask PR11 to form patterns of silicon nitride films 115C (second insulation films).

Detail Description Paragraph - DETX (226):
[0412] Next, ion implantation is carried out to introduce an n-type impurity, i.e., arsenic (As) into the p-wells 5a, 5b and 5c such that the impurity is defined by the SiO.sub.2 films 15a and 15b (first insulation films) and the SiO.sub.2 films 15c (second insulation films), respectively. For example, the ion implantation is carried out with an acceleration energy at 60 KeV and in a dose of 3.times.10.sup.15 atoms/cm.sub.2. As a result of the ion implantation, the impurity is introduced also into each of the gate electrodes 9b and 9e. That is, n-gate (gate electrode of the n-type conductivity) NMOSs are provided.

Detail Description Paragraph - DETX (229):

[0415] An opening on the second mask PR12 in the PMOS-forming region of the low withstand voltage MIS portion is configured in an opening pattern in which the ends of opening are located above the device isolating regions 2 with some margin. The ends of openings of the second pattern mask PR12 in the PMOS-forming region of the high withstand voltage MIS portion are offset from the ends of gate electrode 9a in order to provide a high withstand voltage MISFET having an offset structure.

Detail Description Paragraph - DETX (230):

[0416] Anisotropic etching is carried out on the SiO.sub.2 film 115 using the second mask PR11. As a result, the film is removed from the top of the gate electrode 9a, and side wall films 15d (third gate insulation films) are left on the side walls of the gate electrode 9a. The SiO.sub.2 film 115 is selectively etched on the side walls of the gate electrode 9c with the second pattern mask PR12 to form patterns of SiO.sub.2 films 11 5e (fourth insulation films).

Detail Description Paragraph - DETX (231):

[0417] Next, ion implantation is carried out to introduce a p-type impurity, i.e., boron (B) into the n-wells 4a and 4b such that the impurity is defined by the SiO.sub.2 films 15d (third insulation films) and the SiO.sub.2 films 115e (fourth insulation films), respectively. For example, the ion implantation is carried out with an acceleration energy at 10 KeV and in a dose of 3.times.10.sup.15 atoms/cm.sub.2. As a result of the ion implantation, the impurity is introduced also into the gate electrode 9a. That is, a pgate (gate electrode of the p-type conductivity) PMOS is provided.

Detail Description Paragraph - DETX (234):

[0420] Subsequently, a metal suitable for silicidation to reduce resistance (a refractory metal) is deposited on the principal surface of the semiconductor body 1. Cobalt (Co) is used as such a metal and is deposited to a thickness in the range from about 7 to 10 nm using sputtering. Titanium (Ti) may be used instead of cobalt.

Detail Description Paragraph - DETX (235):

[0421] The deposited cobalt is subjected to an annealing process at 500.degree. C. for about one minute in a nitrogen atmosphere. This process silicidizes the surfaces of the gate electrodes 9a, 9b and 9e and the high concentration regions 19s, 19d, 16s, 16d, 20s, 20d, 17s, 17d, 18s and 18d.

After etching to remove unreacted cobalt on the silicon nitride film 15 and the device isolating regions 2, another annealing process is carried out at 700.degree. C. for about one minute in a nitrogen atmosphere. As a result, metal-semiconductor layers made of cobalt silicide (CoSi2) are formed. The cobalt silicide layers 21s, 21d and 21g are formed only on the surfaces of the exposed semiconductors (gate electrodes and high concentration regions) on a self-alignment basis. Specifically, the salicide layers (cobalt silicide layers 21s, 21d and 21g) are formed in the high concentration regions aligned with the side walls (first and third insulation films) 15a and 15d in the low withstand voltage MIS portion. The salicide layers (cobalt silicide layers 21s, 21d and 21g) are formed in the regions in the sixth embodiment, a high withstand voltage MIS may be formed with such an offset portion on one side thereof (particularly the drain side to which a high withstand voltage is applied). A system LSI includes both of high withstand MISFETS having offset portions on both of those regions and high withstand voltage MISFETS having an offset portion on one of those regions.

Detail Description Paragraph - DETX (236):
[0422] FIG. 61 shows a sectional structure of a high withstand voltage MIS having an offset portion in the drain region thereof according to the present embodiment. While FIG. 61 shows an NMOS, the same structure is employed in a PMOS.

Detail Description Paragraph - DETX (240):
[0426] (2) The invention is characterized in that the gate electrodes of the pair of load PMOSs are formed by a polycrystalline silicon layer including a p-type impurity and a metal silicide layer formed on the surface of the polycrystalline silicon layer and in that the gate electrodes of each of the pair of driving NMOSs and the pair of transfer NMOS5 are formed by a polycrystalline silicon layer including an ntype impurity and a metal suicide layer formed on the surface of the polycrystalline silicon layer.

Detail Description Paragraph - DETX (241):
[0427] (3) As described in the third embodiment, according to the invention, there is provided a semiconductor integrated circuit device in which a first insulated gate field effect transistor for a high withstand voltage and a second insulated gate field effect transistor for a low withstand voltage are

formed in a semiconductor substrate, characterized in that:

Detail Description Paragraph - DETX (242):
[0428] the gate electrode of the first transistor is constituted by a polycrystalline silicon layer, an insulation film being formed on the surface of the polycrystalline silicon layer;

Detail Description Paragraph - DETX (243):
[0429] a metal silicide layer is formed on a high concentration region of each of the source and drain regions of the first transistor;

Detail Description Paragraph - DETX (244):
[0430] the gate electrode of the first transistor is constituted by a polycrystalline silicon layer, a metal silicide layer being formed on the surface of the gate electrode, side wall layers made of an insulating material being formed on side walls of the gate electrode; and

Detail Description Paragraph - DETX (245):
[0431] a metal silicide layer is formed on the surface of a high concentration region of each of the source and drain regions of the second transistor in alignment with the side wall layers.

Detail Description Paragraph - DETX (248):
[0434] (6) As described in the first embodiment, according to the invention, there is provided a semiconductor integrated circuit device in which a first insulated gate field effect transistor for a high withstand voltage and a second insulated gate field effect transistor for a low withstand voltage are formed in a semiconductor substrate, characterized in that:

Detail Description Paragraph - DETX (249):
[0435] the gate electrode of the first transistor is constituted by a polycrystalline silicon layer, an insulation film being formed on the top and lateral surfaces of the polycrystalline silicon layer;

Detail Description Paragraph - DETX (250):
[0436] each of the source and drain regions of the first transistor is constituted by a high concentration region and a low concentration region;

Detail Description Paragraph - DETX (251):
[0437] the insulation film is provided with an opening located above the surface of the high concentration region in each of the source and drain regions of the first transistor;

Detail Description Paragraph - DETX (252):
[0438] a metal silicide layer is formed on the surface of the high concentration region in the opening; the gate electrode of the second transistor is constituted by a polycrystalline silicon layer, a metal silicide layer being formed on the surface of the polycrystalline silicon layer, side wall layers made of an insulating material being formed on side walls of the gate electrode;

Detail Description Paragraph - DETX (253):
[0439] each of the source and drain regions of the alignment with the second side wall layers.

Detail Description Paragraph - DETX (254):
[0440] (8) As described in the first embodiment, the invention is characterized in that the first and second side wall layers are formed at separate steps and in that the metal silicide layers on the surface of the source and drain regions of the first transistor in alignment with the first side wall layers and the metal silicide layers on the surface of the source and drain regions of the second transistor in alignment with the second side wall layers are formed at the same step.

Detail Description Paragraph - DETX (255):
[0441] (9) As described in the sixth embodiment, the invention is characterized in that the first and second side w all layers are formed at the same step and in that the metal silicide layers on the surface of the source and drain regions of the first transistor in alignment with the first side wall layers and the metal silicide layers on the surface of the source and drain regions of the second transistor in alignment with the second side wall layers are formed at the same step.

Detail Description Paragraph - DETX (257):
[0443] (1) According to the invention, a second region (high concentration region) of a first MISFET and a metal-semiconductor reaction layer are aligned with a first gate insulation film; a fourth region (high concentration region)

of a second MISFET and a metal-semiconductor reaction layer are aligned with a second insulation film; and the resistance of electrode extraction portions of the second and fourth regions is reduced by the metal-semiconductor reaction films. This makes it possible to provide a semiconductor integrated circuit device incorporating fine MISFETs capable of a high speed operation.

Detail Description Paragraph - DETX (258):
[0444] Especially, the first insulation films formed on the side walls of the first gate electrode and the second insulation films formed on the side walls of the second gate electrode have different widths in the direction of the gate length, which makes it possible to provide MISFETs having different device characteristics. Specifically, since the width of the second gate insulation films is greater than the width of the first gate insulation films, the distance from an end of a p-n junction formed by a second semiconductor (second well) and a first region to the metal-semiconductor reaction layer is greater than the distance from an end of a p-n junction formed by a first semiconductor (first well) and a second region to the metal-semiconductor reaction layer. This makes it possible to allow a depletion layer to spread in a third region sufficiently and to thereby provide a second MISFET having a withstand voltage higher than that of a first MISFET, i.e., a MISFET which can be driven at a high voltage.

Claims 1 to 9, **insofar as claim 6 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Watanabe (U.S. Patent # 6,048,792).

1. Watanabe (figures 1A to 7C) specifically figure 1B show a semiconductor device comprising: a semiconductor substrate **11**; an active element structure **13,14** formed on the semiconductor substrate, and having a connection region formed in the surface of the semiconductor substrate; a first insulating film **15A** provided on the semiconductor substrate; a contact hole **16** extending from a surface of the first insulating film to the connection region; a contact plug **20** provided in the contact hole; and a buried conductive film **21 or 19** filled in a clearance formed in the contact plug, consisting of a material different from the contact plug, and having a continuous surface without forming a step with the surface of the contact plug.

2. The device according to claim 1, Watanabe further comprising: a barrier metal **19** provided in an interconnect trench formed on the contact plug and the buried conductive

film, and having a bottom surface common to the upper surface of the contact plug and the buried conductive film; and an interconnect layer provided in the interconnect trench, and consisting of a conductive material.

3. The device according to claim 1, Watanabe further comprising: a first intervention conductive film **19** interposed between the inner surface of the contact hole and the contact plug.

4. The device according to claim 3, Watanabe show wherein the buried conductive film **19** and the first intervention conductive film **19** consist of substantially the same material.

5. The device according to claim 4, Watanabe show wherein the buried conductive film **19** and the first intervention conductive film **19** consist substantially of a material selected from the group consisting of TiN and TiSiN or a combination thereof.

6. The device according to claim 3, Watanabe show wherein the first intervention conductive film **19** consists substantially of a material selected from the group consisting of Ti, **TiN** and TiSiN or a stacked film containing a combination thereof, and the buried conductive film consists substantially of a material selected from the group consisting of TiN, TiSi,N, Ta and TaN or a stacked film containing a combination thereof.

7. The device according to claim 2, Watanabe show wherein a film thickness of the first intervention conductive film **19** is equal to or less than 10% of the width of cross section of the interconnect trench.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. The device according to claim 1, Watanabe show wherein the active element structure includes a transistor **13.14**.

9. The device according to claim 1, Watanabe show wherein the contact plug **20** consists substantially of W.

Therefore, it would have been obvious to one of ordinary skill in the art to use the **buried conductive film; first intervention conductive films; and an interconnect trench** as "merely a matter of obvious engineering choice" as set forth in the above case law.

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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watanabe; Kenji	Tokyo	N/A	N/A	JP
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9) FIGS. 1A and 1B show a process for the blanket technique, and FIG. 2 is a timing chart for introduction of gases during the process. In FIG. 1A, a gate electrode 14 is formed on a silicon substrate 11 with an intervention of a gate insulator film not shown, followed by ion-implantation into the substrate 11 to form diffused regions 13 for source and drain. Then, an interlayer dielectric film 15A made of boron-doped phospho-silicate glass (BPSG), followed by patterning to form a via-hole 16 on the diffused regions 13. Subsequently, a Ti--Ni barrier metal layer 19 and a silicon layer 23 are consecutively deposited on the entire surface, wherein the silicon (Si) film 23 is deposited by thermal decomposition of SiH.sub.4, as shown in FIG. 1A, during time interval between ts1 and ts2 as shown in FIG. 2, the silicon film 23 serving for prevention of leakage current in the semiconductor device.

(10) Next, SiH.sub.4 and WF.sub.6 gases are introduced into the chamber, during time interval between t1 and t2 in FIG. 2, to form a first CVD tungsten film 20 having an excellent adhesiveness, followed by deposition of a second CVD tungsten film 21 having a larger thickness to fill the via-holes 16, using H.sub.2 and WF.sub.6 gases during time interval between t3 and t4. The H.sub.2 gas provides a higher deposition rate for the second tungsten film 21 compared to SiH.sub.4 gas. Thereafter, the first and second tungsten films 20 and 21 are etched-back to expose the Ti--Ni barrier films 19, followed by deposition of Al film 22 on the entire surface. The Al film 22 and Ti--Ni film 19 are then patterned to achieve Al

interconnects 22 which are connected to diffused region 13 via tungsten films.

(11) FIG. 3 shows another conventional blanket technique, wherein the tungsten film is deposited on an underlying interconnect layer to form tungsten plug within the via-holes. In this process, via-holes are formed on a first Al interconnect layer 25 overlying a silicon substrate 11. Then, an interlayer dielectric film 15A made of BPSG is formed on the entire surface, followed by patterning thereof to form via-holes exposing therethrough the underlying interconnects 25.

(12) Next, Ti--Ni film 19, Si film 23, first tungsten film 20, second tungsten film 21 and overcoat layer are consecutively formed, as the first conventional case.

(13) The conventional blanket processes for the tungsten film have disadvantages that particles are formed in the tungsten films, which causes a short-circuit failure in the semiconductor device, that a large contact resistance is formed between the tungsten film and the underlying interconnects to degrade the reliability of the semiconductor device, and that the throughput is relatively low.

(2) Now the present invention is more specifically described byway of preferred embodiments thereof with reference to the accompanying drawings.

(3) Referring to FIG. 4A, a transistor element having diffused regions 13 for source and drain and a gate electrode 14 is first formed on a silicon substrate 11 having thereon a field oxide film 12 for separation of the transistor elements. A first interlayer dielectric film 15 made of BPSG is then formed on the entire surface to a thickness of about 200 nm, followed by patterning thereof to form a via-hole 16A exposing a portion of the diffused regions 13.
Subsequently, a sputtering and metallizing process is effected to form a 50-nm-thick tungsten silicide film 17, followed by patterning the same to leave the tungsten silicide film within the via-hole 16a, thereby obtaining the structure shown in FIG. 4A.

(4) Subsequently, a second interlayer dielectric film 18 made of, for example, boron-silicate glass (BSG) is formed on the entire surface to a thickness of 500 nm to 1 .mu.m, followed by

patterning thereof to form a second via-hole 16B aligned with the first via-hole 16A. Thereafter, a metallizing technique is effected to the device at a temperature between 300.degree. C. and 400.degree. C., an ambient pressure between 3 mTorr and 5 mTorr, and an acceleration power between 2 kW and 3 kW to form a Ti--Ni film 19 on the entire surface to a thickness between 100 nm and 150 nm, as shown in FIG. 4B.

(5) Next, a first low pressure CVD (LPCVD) process is effected using WF.sub.6 /SiH.sub.4 gases at a flow rate ratio of 1 to 2 therebetween, with the temperature between 400.degree. C. and 500.degree. C., ambient pressure between several Torr and several tens of Torr, to obtain an about 50-nm-thick first tungsten film 20 on the entire surface. Referring to FIG. 5 showing introduction of gases in the first LPCVD process, SiH.sub.4 gas and WF.sub.6 gas are simultaneously introduced into the CVD chamber at (time instant) t1 and simultaneously stopped for introduction at t2. Then, a second LPCVD process is effected using WF.sub.6 /H.sub.2 gases, with the flow rate ratio therebetween selected at 0.1 to 0.2, temperature between 400.degree. C. and 500.degree. C., pressure between 80 Torr and 120 Torr, to thereby deposit a second tungsten film 21 having a thickness between 0.5 .mu.m and 1.0 .mu.m and filling the second via-hole 16B. By this step, the structure shown in FIG. 4C is obtained.

(6) As shown in FIG. 5, the deposition of the second tungsten film is effected during the time interval between t3 and t4 while introducing WF.sub.6 gas and H.sub.2 gas simultaneously. In this case, however, the starting and stopping of introduction of WF.sub.6 gas and H.sub.2 gas need not be effected simultaneously.

(7) Next, the second tungsten film 21 and the first tungsten film 20 are etched until the Ti--TiN film 19 is exposed as shown in FIG. 4D. Thereafter, an Al film is deposited by a sputtering or metallization technique, followed by patterning thereof by a photolithographic and etching technique to form an Al interconnects.

(8) In the first embodiment, the excess amount of SiH.sub.4 is prevented by introduction of WF.sub.6 gas simultaneously with the introduction of SiH.sub.4 gas, the excess amount of SiH.sub.4 gas in the mixture of WF.sub.6 and SiH.sub.4 gases causing vapor deposition of silicon or tungsten crystals

forming undesirable particles. By our experiments, the first embodiment achieved a 15% reduction of particles during deposition of the tungsten films compared to the conventional process. This configuration also achieved a 5% improvement of the throughput in the deposition of the tungsten films by removing the time interval for introduction of SiH.sub.4 alone.

(9) FIG. 6 shows another timing chart for showing a second embodiment of the present invention, wherein introduction of WF.sub.6 gas is effected at t1 before introduction of SiH.sub.4 gas at t11 during the deposition step for the first tungsten film, and the introduction of WF.sub.6 gas is stopped simultaneously with the stopping of the SiH.sub.4 gas. The other configuration of the second embodiment is similar to the first embodiment, and accordingly, detailed description for the second embodiment is omitted here for avoiding a duplication.

(10) The second embodiment also achieved a 5% improvement in the throughput as well as a 20% reduction of particles compared to the conventional process.
The second embodiment has an additional advantage in that the delayed introduction of SiH.sub.4 assures for prevention of excess amount of SiH.sub.4 gas even if time delay occurs for the flow rate of WF.sub.6 gas reaching at the desired rate.

(11) FIGS. 7A to 7C consecutively show a process steps of a method according to a third embodiment of the present invention.

(12) A first interconnect layer 25 made of Al is deposited on an insulator film 24 made of BPSG formed on a silicon substrate 11. Then, an about 1-.mu.m-thick interlayer dielectric film 15A made of BPSG is formed on the entire surface, followed by patterning the same to form a via-hole 26 exposing therethrough a portion of the first interconnect layer 25, as shown in FIG. 7A.

(13) Subsequently, a first LPCVD process is effected using WF.sub.6/SiH.sub.4 gases to deposit a thin, first tungsten film 20, followed by a second LPCVD process using WF.sub.6 /H.sub.2 gases to form a thick, second tungsten film 21 having a thickness between 0.5 .mu.m and 1 .mu.m. The timing for introduction of WF.sub.6 gas and H.sub.2 gas is similar to that shown in FIG. 5 or 6, and same applies to the other conditions of the CVD process.

(14) Next, an etch-back technique is effected to the first and second tungsten films 20 and 21 to leave a tungsten plug made of the first and second tungsten films 20 and 21 within the via-hole 26. An Al film is then sputter-deposited on the entire surface, followed by patterning the same to form a second layer Al interconnects 22.

(15) The configuration of the third embodiment can achieve a 15% or 20% reduction in particles compared to the conventional process.

(16) Back to FIG. 2 showing the timing chart in the conventional process, the introduction of SiH.sub.4 during the time interval between ts1 and ts2 for Si film formation for reducing the leakage current enlarges the length of time for the heat treatment applied to the semiconductor device by the length of the time interval itself. The deposition temperature for the tungsten is as high as around 400.degree. C. to 500.degree. C. to cause the first layer interconnects underlying the Ti--Ni film to melt and protrude toward the Ti--Ni film in the shape of pin, thereby degrading the reliability in the interconnects. The present invention solves the problem in the conventional technique.

(17) Although the present invention is described bay way of preferred embodiments thereof, the present invention is not limited to the described embodiments and various alterations or modifications can be easily made by those skilled in the art without departing from the scope of the present invention.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/758,774,773,758,301,505,303,748,304,762,764,767,766	3/11/05
Other Documentation: foreign patents and literature in 257/758,774,773,758,301,505,303,748,304,762,764,767,766	3/11/05

Electronic data base(s): U.S. Patents EAST	3/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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